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Modulation Design and Control for Bidirectional Converters in Energy Storage Applications

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***Abstract*— Power converters for energy storage applications employs bidirectional DC-DC converters to achieve high-efficiency power transfer with galvanic isolation. The high-frequency dual active bridge (DAB) DC-DC converter design is particularly sensitive to pulsewidth modulation (PWM) signal mismatches, layout issues, and modulator control asymmetries during dynamic operation. These issues can cause DC offsets in transformer currents, leading to transformer core saturation, distorted current waveforms, and converter premature activation of protection mechanisms.**

The design specifics of the modulator and control are analyzed, incorporating instantaneous balancing of on-time and off-time by adjusting the switching frequency. The modulator is designed to execute smooth phase adjustment using linear ramps while keeping the on-off balanced. Slope compensations are introduced independently between outer and inner phase-angles with ramp limiters. The performance of the proposed design is evaluated during bidirectional power flow transitions in both charge and discharge modes. The experimental results are performed using a 5 kW nominal power bidirectional DC-DC converter with silicon carbide devices.

Keywords*— *Dual active bridge, modulator design, phase-shift control.

I. Introduction

Recent applications, such as electric vehicle chargers and solar photovoltaic systems, require the integration of advanced power electronic topologies and control strategies with energy storage solutions. The wide voltage operational range remains a challenge in conventional resonant converters, while the dual-active bridge (DAB) converter can be designed to accommodate a broader voltage range. Residential and commercial energy storage systems, on-board EV chargers can be designed with AC-DC power factor correction (PFC) and isolated DC-DC converters as shown in Fig. 1. DC-DC DAB isolated converters offer significant advantages, including bidirectional power flow, soft-switching operation, and high power density ([1-3]). The challenges associated with achieving zero voltage switching (ZVS), managing reactive power due to circulating currents, and implementing pulsewidth modulation (PWM) control in the DAB converter have been explored in previous studies ([4-5]).

New DAB topologies featuring series high-voltage and parallel low-voltage for higher current operation, wide voltage operation and extended power capability have been recently explored ([6-9]).

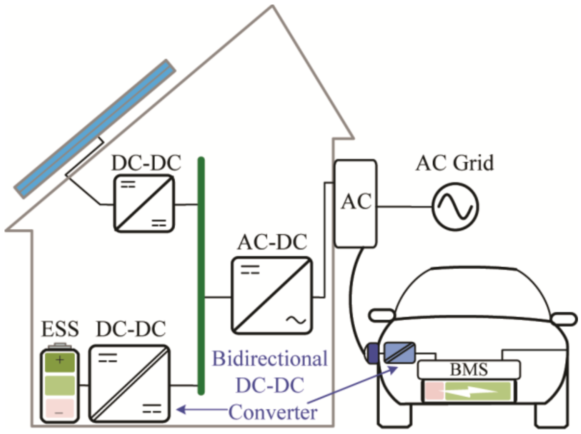

Fig. 1. Typical application of bidirectional DC-DC converters.

DC offsets in volt-seconds are present in the inputs on either side of the transformer, and they can cause DC currents to flow through the transformer. This phenomenon has posed a significant challenge for both isolated converters and utility-scale transformers.

The issues of DC offset issues have been investigated with methods of detecting DC bias in transformer. Active control of DC offsets can be implemented controlled through directly measuring the primary and secondary transformer currents and through analysis of the flux or the saturation in the transformer core [10-12]. These methods require additional measurement hardware while increases the control efforts.

In this paper, the proposed modulator is designed with the following features: on-time and off-time balancing through the adjustment of the switching frequency, low-jitter design and independent outer and inner phase angle control with slope compensation.

The proposed modulation design methodology is introduced in Section II, with the investigation of key details of the modulation control, phase-angle gradient compensation. The experimental validation of the bidirectional DC-DC converter design methodology are presented in Section III, followed by the concluding remarks in Section IV.

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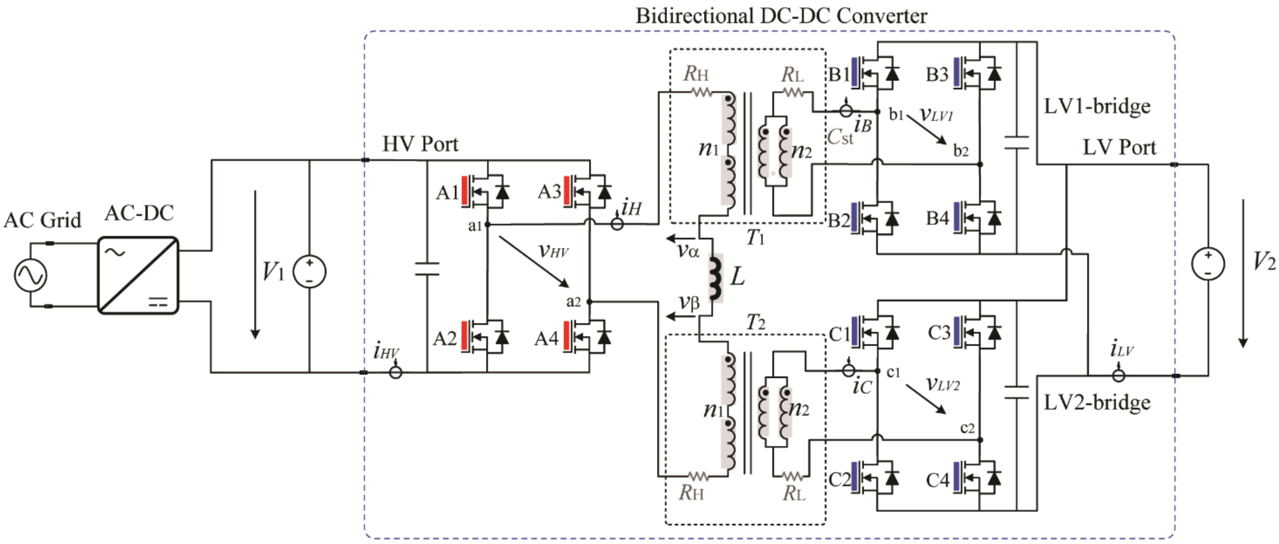

Fig. 2. Energy storage system diagram: AC-DC converter and DC-DC DAB converter for bidirectional energy conversion.

II. Proposed Modulator design for the bidirectional DC-DC converters

Fig. 2 illustrates the topology of the parallel-series DAB bidirectional DC-DC converter. The DAB converter has been extended to include three full-bridge converters. To accommodate the high currents on the low-voltage (LV) side, the bridge is divided into two channels, with each channel managing half of the rated power.

The current sharing of each LV bridge must be ensured to avoid volt-second imbalances of transformers T_1 and T_2, which can cause magnetics saturation. The high-voltage secondaries of transformers T_1 and T_2 are series connected as shown in Fig. 2. The inductor L, which allows the power flow control, interconnects the series secondaries to the HV bridge.

To prevent volt-second imbalances in transformers T_1 and T_2, which could lead to magnetic saturation, proper current sharing between the LV bridges must be maintained. The high-voltage secondaries of T_1 and T_2 are connected in series, as depicted in Fig. 2. The inductor LL, responsible for facilitating power flow control, links the series-connected secondaries to the HV bridge.

As shown in Fig. 2, the voltage impressed over the power inductor $v_L(t)$ with the inductor current (i_H) delivered during each switching period (T) is given by

$$v_L(t) = v_\alpha(t) - v_\beta(t) = L\frac{di_H(t)}{dt}. \tag{1}$$

The total average active power (P) generation during one switching period (T) is given by the sum of the two LV-bridges,

$$P = \frac{1}{T}\left[\int_0^T p_1(t)\,dt + \int_0^T p_2(t)\right]dt, \tag{2}$$

where $p_1(t) + p_2(t) = p(t)$ is the active power delivered from the two LV-bridge converters. The average power delivered during charge and discharge can be characterized by the contributions from the LV1 and LV2 bridges,

$$\begin{cases} P_{\text{charge}} = \frac{1}{T}\int_0^T v_\beta(t)i_{\text{H}}(\text{t})\,dt \\ P_{\text{discharge}} = \frac{1}{T}\int_0^T v_\alpha(t)i_{\text{H}}(\text{t})\,dt. \end{cases} \tag{3}$$

With the consideration of the phase-shift, the calculated active power transfer in charge and discharge of the bidirectional converter is given by

$$P = nV_1V_2\frac{1}{2\pi fL}\delta\left(1 - \frac{|\delta|}{\pi}\right). \tag{4}$$

where $n = (2n_1)/n_2$ is the transformer (T_1, T_2) turns-ratio.

Equation (4) defines the relationship between the active power transferred and the phase-shift (δ) between the HV and LV bridges, the converter's switching frequency, and the energy transfer inductance. The single phase-shift (SPS) control method simulataneously turns-on and -off the diagonal switches in each full-bridge converter with 50% duty ratio. The dead time (T_d) is introduced to elinimate an accidental the cross-conduction of the switches operating of the same leg. The deadtime is introduced while maintaining time-on and -off equal within the same period The period calculation must satisfy at the moment of the switching period (k) the following

$$\begin{cases} T_{(\text{k})} = T_{\text{on(k)}} + T_{\text{off(k)}} + 2T_{\text{d(k)}} \\ T_{\text{on(k)}} = T_{\text{off(k)}} \end{cases}$$

The PWM timing for one of the four channels is illustrated in Fig. 3. All four channels have the same on time, dead time, and switching frequency. However, during dynamic phase changes, on/off time and the overall PWM period duration shall vary temporarily, in order to satisfy relation (5).

Fig. 4 shows the converter waveforms operation with TPS control. The HV-bridge is controlled by PWM A1/A2 and PWM A3/A4, LV1-bridge and LV2-bridge are simultaneously controlled by PWM B1/C1, PWM B2/C2, PWM B3/C3 and PWM B4/C4. The phase-shit δ controls the bidirectional power transfer between the source and the load.

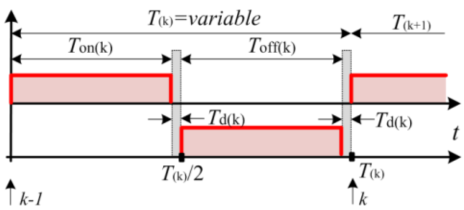

Fig. 3. PWM generation for complementary switches.

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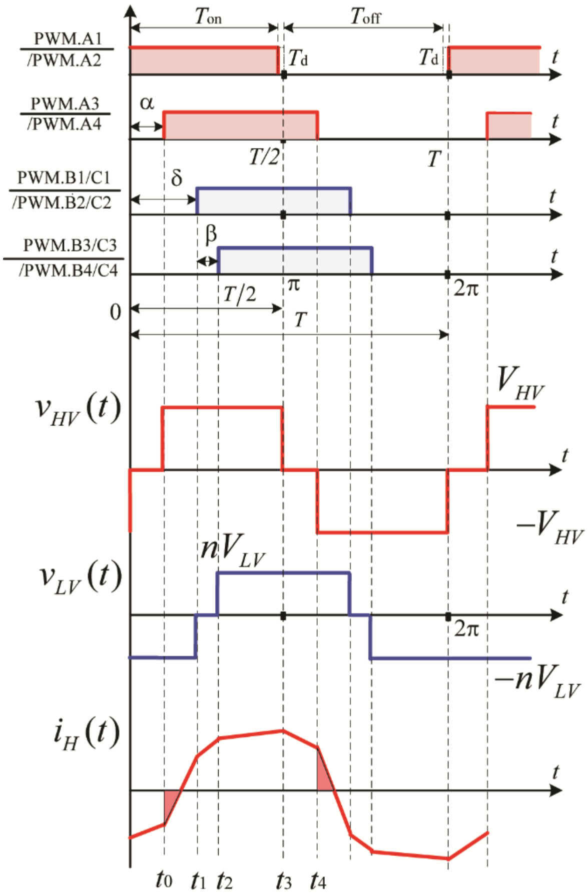

Fig. 4. Key operational waveforms with triple phase-shift modulation example in charge mode.

The inner phase-shifts, α and β, are implemented in the HV bridge and the LV1/2 bridges, respectively, to enhance soft-switching and improve conversion efficiency. As shown in Fig. 4, the HV-bridge voltage v_{HV} leads v_{LV} which determined the power transfer from high-voltage (HV) bus to low-voltage (LV) battery port.

Fig. 5 illustrates the design and implementation of the control strategy for the parallel-series configuration of the LV-bridges.The main controller defines the reference set-points for the voltage, with v_1^* for discharge and v_2^* for charge, and the current i_1^* for discharge and i_2^* for charge mode of operation. The voltage and current regulators, $G_v(s), G_i(s)$, control the outer phase-shift (δ) between the HV-bridge and the LV-bridges to regulate power flow from the source to the load.

The inner phase-shifts α and β, are utilized to extend soft-switching, thereby achieving higher conversion efficiency. The two-level voltage switching waveforms, controlled by the single phase-shift (δ), can be converted into three-level voltage modulation ($v_\alpha(t), v_\beta(t)$) by using triple phase-shifts (δ, α, β).

The PWM generator produces four pairs of PWM signals, each pair forming a complementary channel. In this work, each channel is designed to operate at constant switching frequency which is equal among the channels, and each channel features a fixed dead-time. The dead-time is a critical window of time during which neither transistor of a pair is on, to avoid undesired shoot-through. The dead-time has been selected as a hard-coded property, does not vary, and is determined from circuit analysis of the connected bridge elements. The two transistor on-times in a channel alternate in a complementary fashion, and they are equal and balanced. The phases of the 4 PWM channels are defined relative to the A1/A2 PWM channel. The PWM generator is synchronized with a master period control from which the individual phases are derived. All PWM channels, including A1/A2, are set relative to the internal master. The phase setting is an unsigned number and the negative values are not allowed, where the phase setting should be rounded to the nearest integer. The PWM phase expressed as a measure of time and for each increment of the phase setting, the PWM is additionally delayed by one period of the internal digital clock. The outer phase-shift δ and the inner phase-shift α are defined and measured relative to the phase of A1/A2 channel. The second inner phase-shift β is defined and measured relative to the phase of B1/B2 channel. The B3/B4 channel has a phase that is the sum of δ and β, relative to the A1/A2 channel.

This functionality allows for directly setting initial phases without soft-start ramping, prior to activating the PWM generators. It is commonly employed for configuring initial settings following a device power-up or reset and can also be used to implement immediate phase adjustments, whether large or small.

In case of an automatic soft-start and slope compensation, when a phase setting is applied while the generators are active, it serves as the target phase for the corresponding channel, which then automatically ramps its phase to reach the specified target. The phase target for a channel can be updated at any time, even if automatic ramping is still in progress.

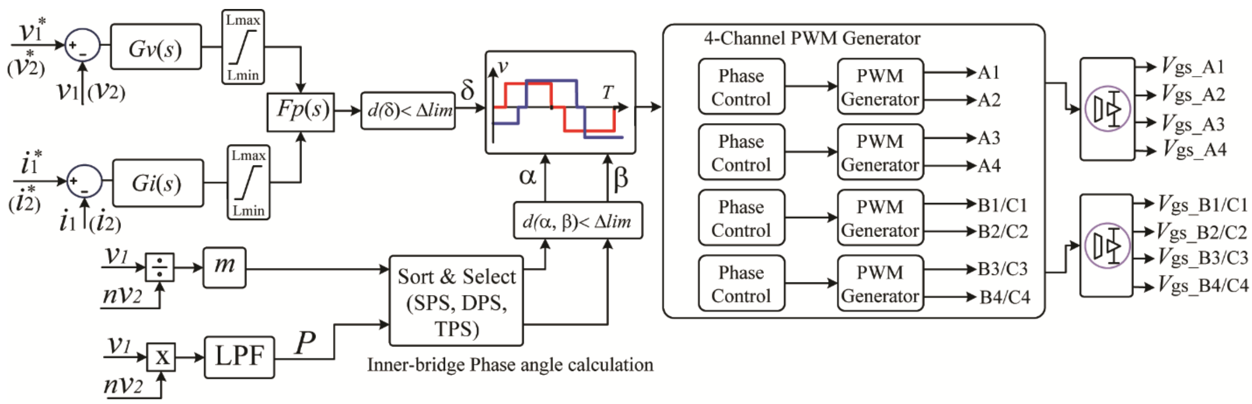

Fig. 5. Proposed modulator design for bidirectional DC-DC converter.

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Applying a new phase setting immediately overrides the previous target and establishes the new target phase. The advantage of the proposed method is that, during dynamic converter operations, the volt-seconds of the transformer voltages are maintained balanced to avoid transformer saturation. In order to avoid transformer saturation due to induced DC components, the PWM generator is further analysed.

The jitter specifications are especially significant as they directly impact the PWM output operation. In this work, an objective is to achieve elimination or extremely low jitter, where the circuit design implies to use of clocks derived from the PLL with an external crystal featured with high tolerance values (ECS-200-20-3X, ±10ppm). The disadvantage of this design approach is that of not using the internal RC type oscillators and adding of external with tight tolerances (±10ppm) components and layout design for signal integrity.

The proposed methodology for direct phase-angle control is through the PWM phase of a channel changed by temporarily adjusting the switching period (T) as shown in Fig. 3. For direct phase-angle control, the on-time for one half-period is adjusted, while maintaining the dead time of the channel. To reduce the phase, the on-time is shortened, while increasing the phase involves lengthening the on-time. These adjustments are made at the tail end of the on-time.

Phase adjustments are applied instantaneously in a step manner. The step-size is internally determined based on the difference between the desired new phase and the current phase of the relevant channel. A single, sufficiently large adjustment—either up or down—is made within one half-period to achieve the target phase. Following this adjustment, the switching periods revert to their nominal length, and the new phase becomes effective. The modulator is designed to automatically execute a phase adjustment as a smooth, linear slope compensation to the desired new phase while keeping the PWM outputs enabled. This process requires only a single phase setting, after which the phase of the relevant channel is gradually ramped to the specified value. When a new phase setting is initiated, the difference between the new phase and the current phase of the channel is continuously calculated throughout the ramping process. During each switching period, the phase is adjusted by this difference. For small differences, the adjustment is applied in a single step, either up or down, equal to the difference. For larger differences, the phase is incremented or decremented by the maximum allowable step size, limiting the adjustment per period. This constraint ensures controlled increasing or reducing of the switching period and the transistor on-time. The proposed slope compensation, as shown in Fig 5, is introduced independently between phase-angles δ, α, β with the following slope limiters,

$$\frac{\mathrm{d}(\propto,\beta,\delta)}{\mathrm{dt}} < \frac{\mathrm{d}(\propto,\beta,\delta)_{\mathrm{lim}}}{T} \quad (5)$$

During phase adjustments with automatic ramping, the phase movement and ramp rate are primarily governed by constraints on the switching period and the on-time of the complementary switches. Both the period adjustment and imbalances between the two on-and off-time intervals within a switching period are restricted by upper and lower limits.

Therefore, during start-up, transients and reverse power transfers, the volt-seconds of the transformer voltages are maintained balanced.

III. Simulation and Experimental results

The problem of the DC offsets can result in current surges which can damage the power devices and compromise system reliability. If the converter is designed with over-current protection, the limiting circuit shut down of the converter when the current reaches transformer core saturation level. Table I shows the main parameters of the DAB converter used in the experimental results.

Fig. 6 shows the key waveforms of the DC-DC bidirectional converter during its operation in charge mode. The implementation of inner phase-angles allows soft-switching commutation for the power devices, therefore operation at high conversion efficiency. The PWM generation waveforms are shown in Fig 6 satisfying the equation from (5).

TABLE I

Main Parameters of the DAB Converter with parallel and series bridge configuration

Parameter	Symbol	Value
Nominal Power	P_n	5 kW
DC Bus	V_1	380 V
Battery Voltage	V_2	48 V
Power Inductor	L	20 µH
Magnetizing Inductance	L_m	1 mH
Switching frequency	f	83 kHz

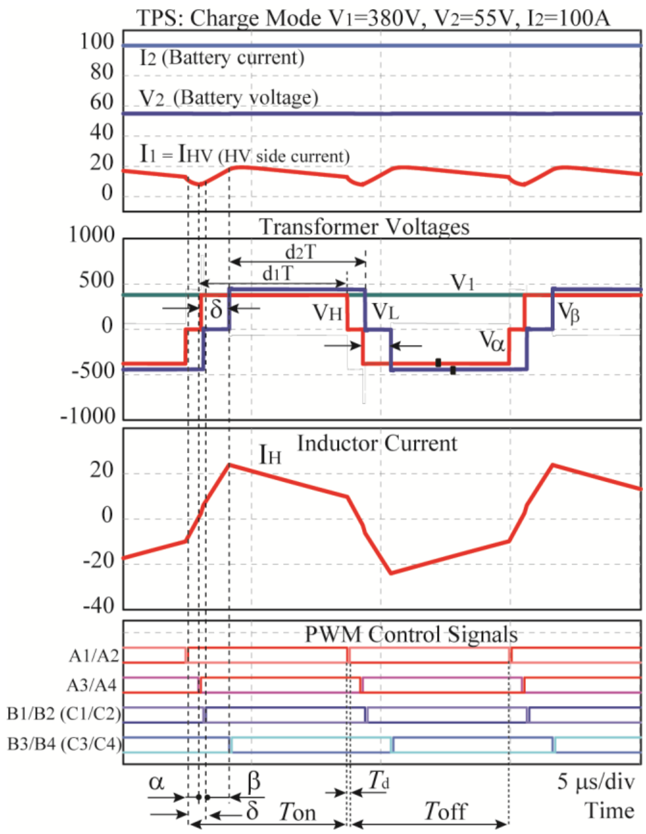

Fig. 6 Simulation results of the bidirectional DC-DC converter operating in charge mode with the applied modulation strategy: $V_1 = 380V, V_2 = 55V, I_2 = 100A, P_1 = 5kW$.

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A. Examples of issues in DAB converters

Fig. 7 shows the converter's gate-to-source voltage experimental waveforms under discharge mode at 5 kW nominal power operations. Layout issues, such as not separating the gate-drive signals from the power switching-traces, can result in noise being induced in the critical gate-source signals.

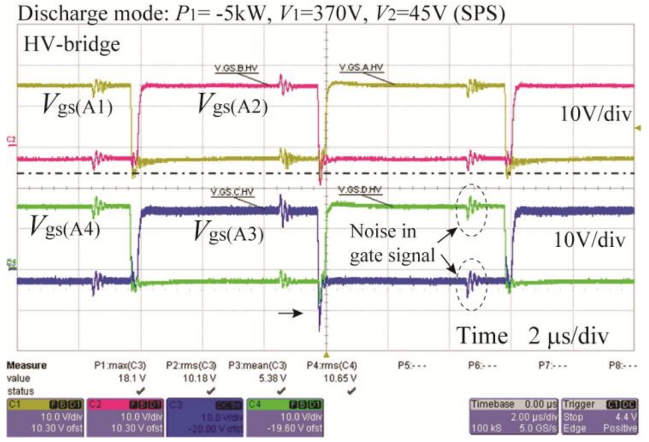
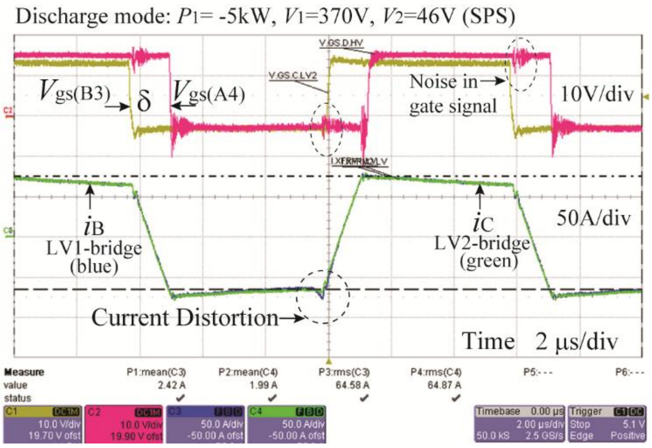
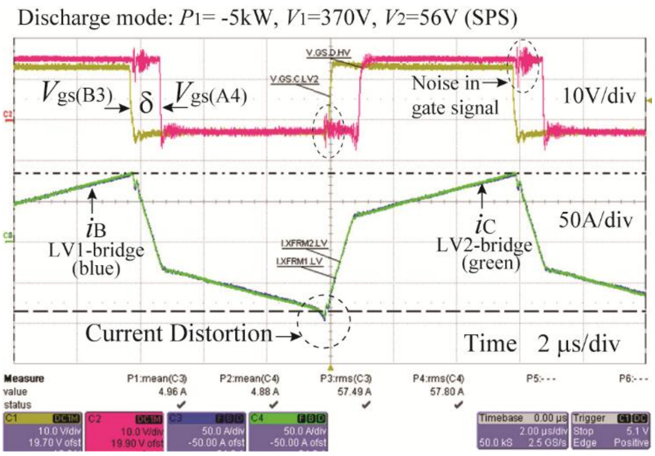


Fig. 7 Experimental waveforms example illustrating issues in DAB converters caused by noise on the gate-source voltage of SiC MOSFETs.



(a) Discharge mode ($V_2 = 46V$)



(b) Discharge mode ($V_2 = 56V$)

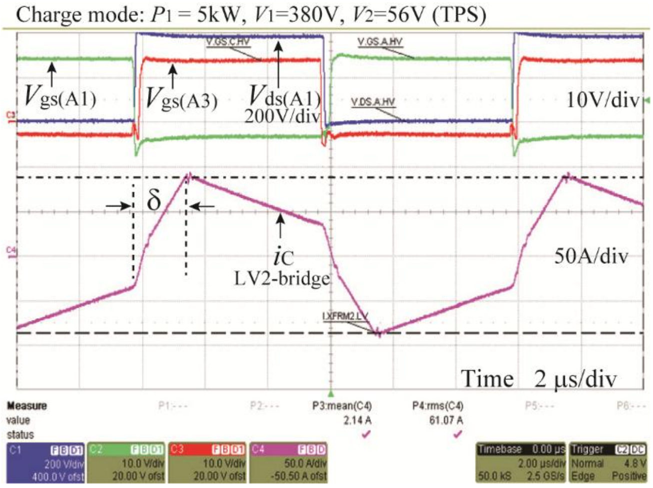
Fig. 8. Transformer DC component with current distortion issues in discharge mode: experimental waveforms. Test conditions: $P_1 = 5kW$, $V_1 = 370V$.

Figs. 8 (a) and (b) show the converter in discharge mode at 5 kW nominal power (at battery voltage 46 V and 56 V, respectively) with undesired noise on the gate-drive signals on the HV-bridge ($e.g., V_{gs}(A4)$) due to layout issues as explained previously. The two transformer currents in the LV1-bridge (i_B) and LV2-bridge (i_C).show signs of transformer saturation, as indicated with the pronounced currents negative peaks. The DC bias in the transformer causes a reduction in relative magnetic permeability (μ_r) which drives the transformer into the saturation region.

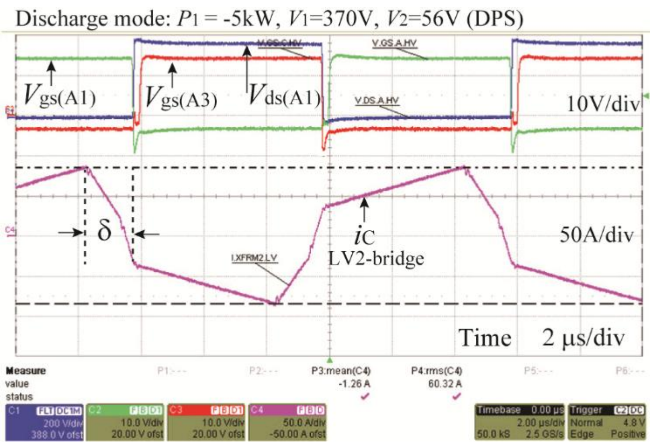
B. DAB converter operation with the proposed modulation and design techniques

Fig. 9 demonstrates the enhanced performance achieved through the proposed modulation and design techniques, as evidenced by the experimental waveforms of the converter operating in steady state at 5 kW and a battery voltage of 56 V.

The tests were performed in charge (a) and discharge (b) modes, with the transformer current (e.g., i_C current in LV2-bridge) showing symmetry and no signs of saturation. The gate-drive signals are free of noise, thanks to layout design. The gate drive signal traces were routed separately from the power traces and switching nodes.



(a) Discharge mode ($V_2 = 46V$)



(b) Discharge mode ($V_1 = 370V$)

Fig. 9. Experimental waveforms of the bidirectional power converter with proposed modulation and design techniques. Test conditions: $P_1 = 5kW$, $V_2 = 56V$.

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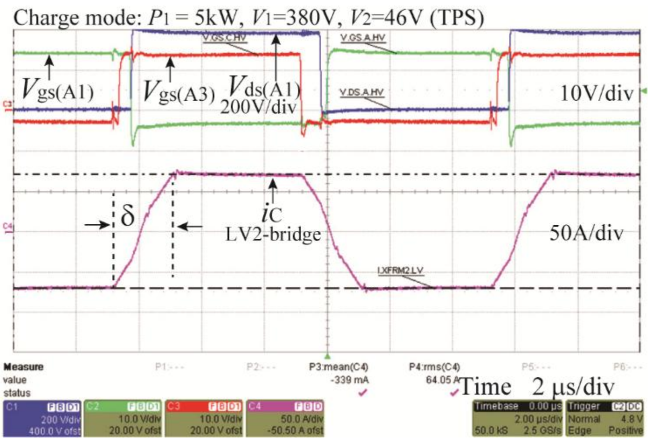
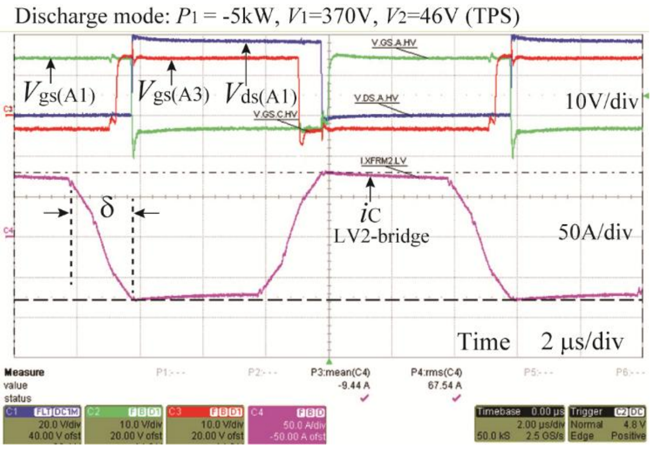
The turn-on and turn-off switching voltage across the power devices, such as $V_{ds(A1)}$, shows an adequate design margin for drain-source overshoots during commutation events, remaining well within the specified safe operating area. Fig. 10 shows another set of tests with improved performance of the DAB converter thanks to the control structure (Fig. 5) and explained design techniques in Section I.
The experimental results were conducted under the test case with 5 kW and 46 V battery voltage.

Fig. 10 (a) shows the HV-bridge gate control signal $V_{gs(A1)}$ part of the first leg, and $V_{gs(A3)}$ part of the second leg with TPS control. The control of the phase-angle δ results in $5kW$ power charge from 380V DC bus to 46 V battery port.



(a) Charge mode ($V_1 = 380V$)



(b) Discharge mode ($V_1 = 370V$)

Fig. 10. Experimental waveforms of the bidirectional power converter using the proposed modulation and design techniques. Test conditions: $P_1 = 5kW, V_2 = 46V$.

IV. Conclusion

The issues of imbalanced voltage-seconds of the transformer voltages can lead to transformer core saturation as shown in the experimental results. Unsupervised design can result in mismatched volt-second signals applied to the series-parallel transformer windings configuration. These discrepancies accumulate during the converter's switching operation, potentially causing significant effects such as the saturation of magnetic components. The proposed modulator and control was designed with symmetrical on-time and off-time balancing through the adjustment of the switching frequency. This modulator was designed to automatically execute a phase adjustment as a smooth, linear slope compensation to the desired new phase while keeping the on-off time balanced. The proposed slope compensation is introduced independently between phase-angles δ, α, β with gradient limiter. As a result, the modulator maintains the balance of voltage-seconds within the primary and secondary transformer windings, as demonstrated in the experimental results.

In summary, the proposed modulator design offers several advantages, including effective mitigation of transformer core saturation through balanced volt-second operation, enhanced soft-switching capabilities that improve converter efficiency, and a low-jitter PWM generation approach that ensures stable and predictable switching performance. The expense of the proposed modulation are related to higher tolerance of few external components and adherence to engineering best practices in layout routing to ensure signal integrity.

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