BENEFITS OF HIGH-SWITCHING FREQUENCY ON DC-LINK CAPACITORS

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Abstract

Commercial and industrial inverters are designed to meet demanding requirements and constraints including cost, volume, weight, reliability, expected lifetime, efficiency and working environment stresses. An essential component in these inverters is the DC-link capacitor, which can impact all these factors. As such, any DC-link enhancement has systemwide implications. This paper demonstrates the positive impacts that increasing the switching frequency has on reducing DC-link ripple current, which can result in cost, volume and weight reductions. Additionally, reduced losses related to ripple current result in longer component life and better efficiency. Hillcrest's new soft-switching technology helps to achieve higher switching frequency without increasing switching losses and electromagnetic interference (EMI), which offers numerous system-level benefits including the aforementioned positive affects on DC-link capacitors.

Introduction

Due to recent energy and carbon emission polices, high-voltage converters have proliferated in markets such as EV traction systems, renewable energy generation and power quality enhancement systems, to name just a few. Each application has unique challenges, requirements, and constraints such as reliability, power density and useful life. One essential part of these converters is the DC-link capacitor bank, which provides a low-impedance voltage source for high frequency currents, acting as a buffer between instantaneous active power of the AC output and the DC source, and decoupling the effects of stray inductance of the DC busbars and cables. These capacitors contribute considerably to the cost, size, and failure rate of a converter. As illustrated in Fig. 1, in an EV traction inverter, DC-link capacitors comprise 14% of total inverter cost [1] and, as depicted in Fig. 2, account for 21% of a 110kW EV traction system inverter's weight [2]. Therefore, any reduction in DC-link capacitor size translates into cost and weight reduction of the converter.

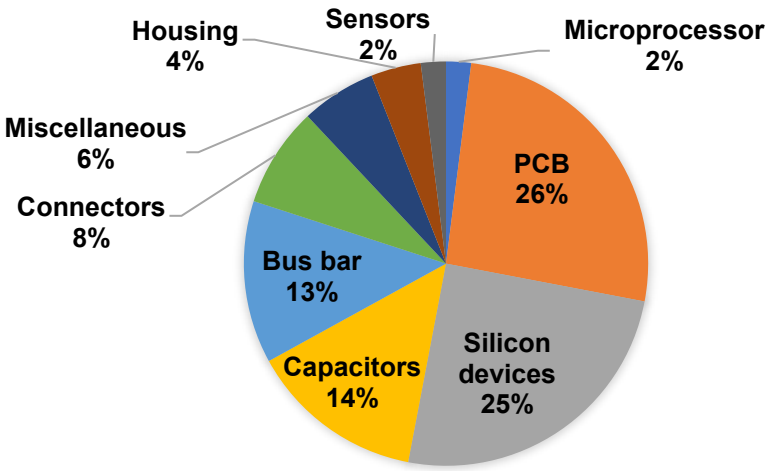

Fig. 1. Cost break-down of a traction inverter.

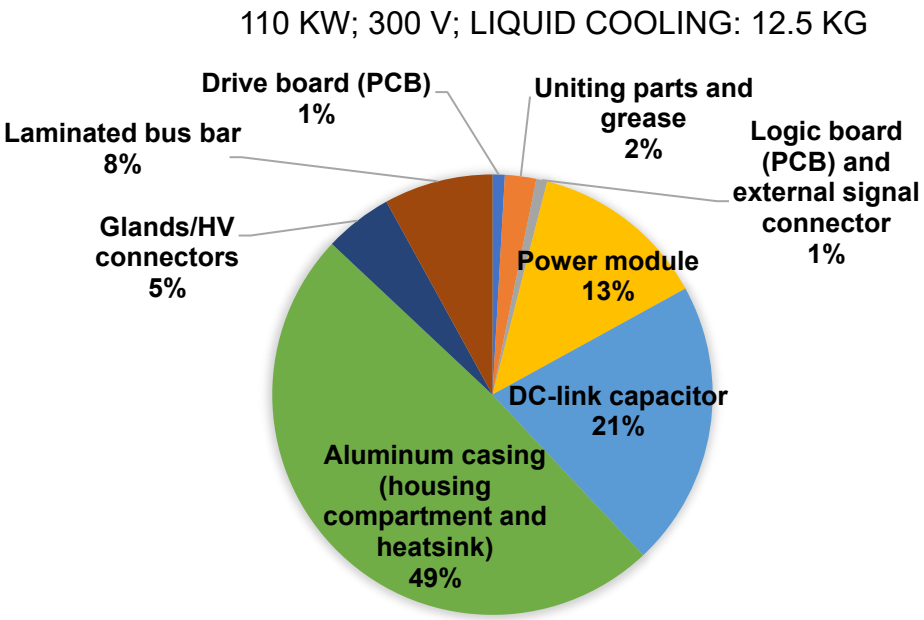

Fig. 2. Weight breakdown of a 110kW traction inverter.

Fig. 3 illustrates the ratio of various faults among power electronic components for a 3-phase, 2-level voltage source inverter such as those used in EV traction systems [3]. As shown, 30% of inverter failures are attributed to capacitors. A similar study in solar power showed that grid inverter failures account for 36% of total energy losses, 7% of which were DC-link capacitor failure [4]. These numbers are highly dependant on the capacitor type; another study found that electrolytic

capacitors can comprise up to 60% of the converter failures [5]. This data reveals that taking measures to improve capacitor life and reliability directly benefits system life and productivity.

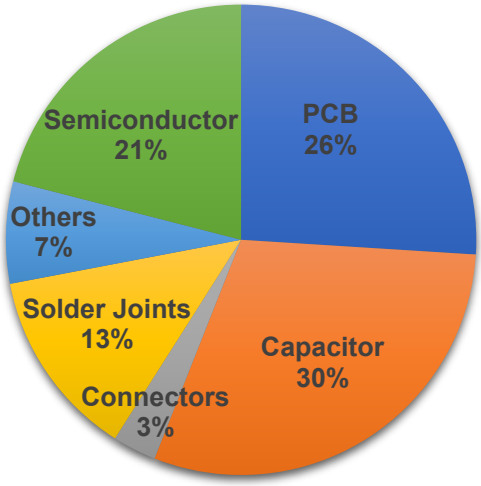

Fig. 3. Distribution of failure rate of a traction inverter.

Capacitor's lifetime empirical model which describes the influence of temperature and voltage is as follows [7]:

$$L = L_0 \times \left(\frac{V}{V_0}\right)^{-n} \times \exp\left[\left(\frac{E_a}{K_B}\right)\left(\frac{1}{T} - \frac{1}{T_0}\right)\right] \quad (1)$$

where L and L_0 are the life under the utilization and test conditions, respectively. V and V_0 are the voltage at utilization and test conditions, respectively. T and T_0 are the temperature in Kelvin at utilization and test conditions, respectively. K_B is Boltzmann's constant (8.62×10−5 eV/K), and n and E_a are the voltage stress exponent and the activation energy, respectively, and their value depends on the dielectric material.

As the empirical model of a capacitor (1) shows, a smaller increase in temperature improves the expected life of the capacitor. To reduce the core temperature, losses in a capacitor should be reduced.

At low frequencies, e.g. 1 kHz, capacitor dielectric losses are dominant, therefore equivalent series resistance (ESR) decreases roughly proportional to the inverse of frequency. At medium to high frequencies, e.g. 100kHz, losses in the conductors are dominant, and ESR becomes relatively constant. At very high frequencies (>10 MHz) ESR increases by the square root of frequency due to the skin effect [6]. ESR variation versus frequency for a film capacitor is shown in Fig. 4. If the frequency can be increased to a more optimal range, losses in the capacitor decrease, which results in a smaller increase in temperature and as a result, improved efficiency and component

lifetime. Further reduction of the losses in the DC-link capacitors is achieved by the capacitor ripple current reduction.

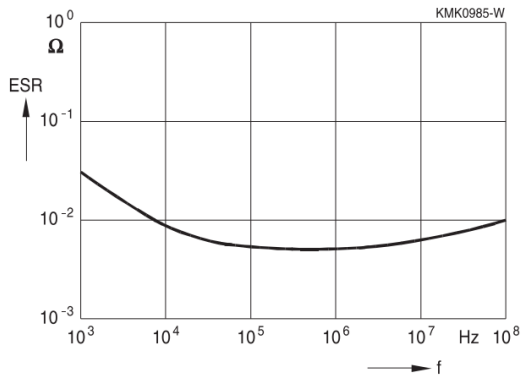

Fig. 4. ESR changes versus frequency.

This paper will show how Hillcrest's inverter technology reduces DC-link capacitor size and losses, while increasing its reliability and service life. In the following section, calculation of the DC-link capacitor's ripple current and its size are explained. Then, experimental and simulation results are shown and discussed to demonstrate the effectiveness of the Hillcrest high-efficiency inverter technology ("Hillcrest inverter technology" and "Hillcrest inverter") in improving DC-link parameters. In this section, a comparison of different switching frequencies is made to quantify the advantages.

DC-Link Capacitor Size Calculation

As discussed previously, DC-link capacitors provide a relatively low AC impedance voltage source. These currents, and thus capacitor high-frequency voltage ripple, are related to switching frequency, modulation method, duty cycle, load power factor and output current amplitude [8]. To optimize DC-link capacitor size, system parameters within which a converter is to be utilized should be determined. For the scope of this paper, only a worst-case scenario of space vector modulation (SVM) is discussed.

SVM is a well-known modulation method utilized in many applications. Fig. 5 shows the SVM switching states of an inverter. To generate a reference voltage, two active switching states along with zero states are used.

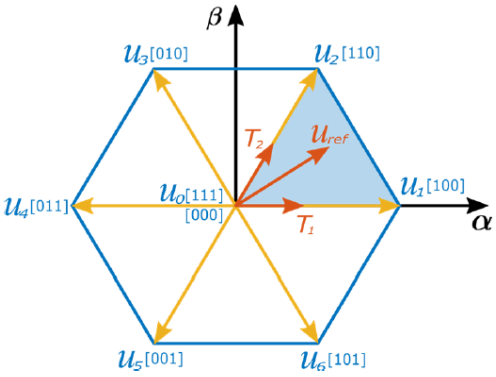

Fig. 5. Space vectors for a converter.

The most common way to switch the power switches is to start the switching string with a zero state and end with a zero state, and only do one switch transition at a time. Fig 6 shows the switching string and how a microcontroller pulse-width modulation (PWM) comparator should be configured in the first sextant. Six sextants of the hexagon are symmetrical; therefore, analysis is only done in the first sextant.

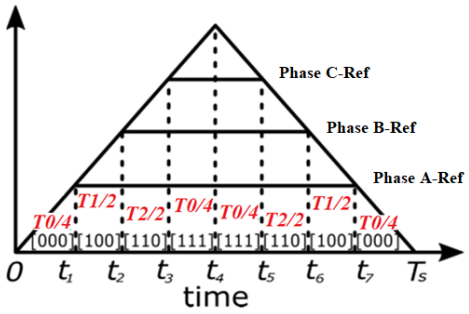

Fig. 6. Timing, comparator values and switching string in first sextant.

With reference voltages as (2), the time for each vector duty cycle can be calculated as (3).

$$\begin{cases} v_a = V_m \cos(\omega t) \\ v_b = V_m \cos\left(\omega t - \frac{2\pi}{3}\right) \\ v_c = V_m \cos\left(\omega t + \frac{2\pi}{3}\right) \end{cases} \tag{2}$$

$$\begin{cases} T_1 = \left(\frac{3}{2}\, m \cos \omega t - \frac{\sqrt{3}}{2}\, m \sin\omega t\right) T_S \\ T_2 = \left(\sqrt{3}\, m \sin\omega t\right) T_S \\ T_0 = \left(1 - \frac{3}{2}\, m \cos \omega t - \frac{\sqrt{3}}{2}\, m \sin\omega t\right) T_S \end{cases} \tag{3}$$

where m is defined as maximum phase voltage over DC-link voltage, which means m_{max}=2/3.

To calculate maximum voltage ripple, capacitor current during each time interval (shown in Fig. 6) must be found first. Load phase voltages and currents are as (2) and (4), respectively.

$$\begin{cases} i_a = I_m \cos(\omega t - \varphi) \\ i_b = I_m \cos\left(\omega t - \varphi - \frac{2\pi}{3}\right) \\ i_c = I_m \cos\left(\omega t - \varphi + \frac{2\pi}{3}\right) \end{cases} \quad (4)$$

The total active power delivered to the load is:

$$P_{3ph} = \frac{3}{2} V_m I_m \cos(\varphi) \quad (5)$$

This power is provided by the DC source; therefore, the DC source current can be calculated as:

$$i_{DC} = \frac{3 V_m I_m \cos(\varphi)}{2 V_{DC}} = \frac{3}{2}\ m\ I_m \cos(\varphi) \quad (6)$$

The current passing through the capacitor (Fig. 7) in each interval is the difference of i_{DC} and i_{cnv} which is a function of load current and switching state. For the first sextant, the current passing through the capacitor (i_C) during each interval is as listed in Table I. As the modulation is symmetrical, the voltage ripple in the next half of the switching period will be same.

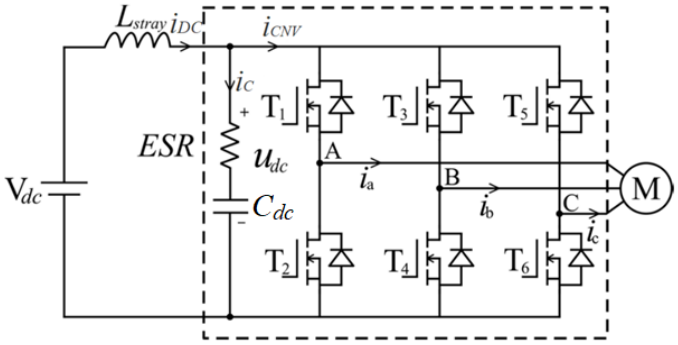

Fig. 7. Structure of a 3-phase, 2-level inverter.

Table I: DC-link capacitor's voltage ripple in each sector of first sextant.

Interval	i_C	Time	Voltage ripple(Δu_{dc})
1	i_{DC}	$T_0/4$	$\frac{3.I_m}{2.C_{dc}} \mathrm{m}\cos\varphi \left(1 - \frac{3}{2}\ m\cos\omega t - \frac{\sqrt{3}}{2}\ m\ sin\omega t\right) T_S/4$
2	i_{DC}-i_a	$T_1/2$	$\frac{I_m}{C_{dc}} \left[\frac{3}{2}\mathrm{m}\cos\varphi - \cos(\omega t - \varphi)\right] \left(\frac{3}{2}\ m\cos\omega t - \frac{\sqrt{3}}{2}\ m\ sin\omega t\right) T_S/2$
3	i_{DC}+i_a	$T_2/2$	$\frac{I_m}{C_{dc}} \left[\frac{3}{2}\mathrm{m}\cos\varphi + \cos\left(\omega t - \varphi + \frac{2\pi}{3}\right)\right] \left(\sqrt{3}\ m\ sin\omega t\right) T_S/2$
4+5	i_{DC}	$T_0/2$	$\frac{3.I_m}{2.C_{dc}} \mathrm{m}\cos\varphi \left(1 - \frac{3}{2}\ m\cos\omega t - \frac{\sqrt{3}}{2}\ m\ sin\omega t\right) T_S/2$

DC-link voltage ripple is linearly proportional to the output current amplitude and switching frequency. The ripple coefficient (shown in red in Table. I) should be solved numerically, with maximums found for the entire span of the modulation index (m) used, and possible load power factor (φ). The full range of m is 0 to 0.57 (without overmodulation). Next, the full range of the power factor and modulation index, as shown in Fig. 8, maximum ripple coefficient is 0.25 for $m = {}^{1}/_{\sqrt{3}}$, $\varphi = {}^{\pi}/_{2}$. Therefore, for the worst case, the DC-link capacitor should be chosen as:

$$C_{dc} > \frac{I_m T_s}{4\Delta u_{dc-max}} \tag{7}$$

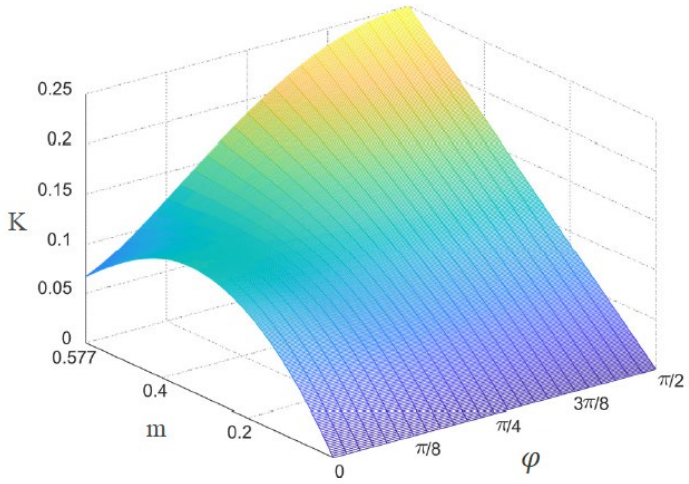

Fig. 8. Maximum ripple coefficient for SVM modulation method in full range of modulation index and power factor.

As illustrated, the DC-link capacitance, in a specific modulation method and defined switching frequency, is a function of amplitude of output current, modulation index and power factor. However, an additional consideration is the current ripple and harmonics of the output current. Formulas above all assume the load current is pure sinusoidal and constant during a switching period (Fig. 9-1). As shown in Fig 9-2 and 9-3, in practice, in many applications, there is a considerable amount of current ripple on the converter side. For example, with grid applications, the acceptable current ripple in the converter side inductor of the LCL filter may be around 30% or more. Therefore, the effect of this ripple current should be considered in the DC-link capacitor calculation which will be a value in addition to the value calculated by (7).

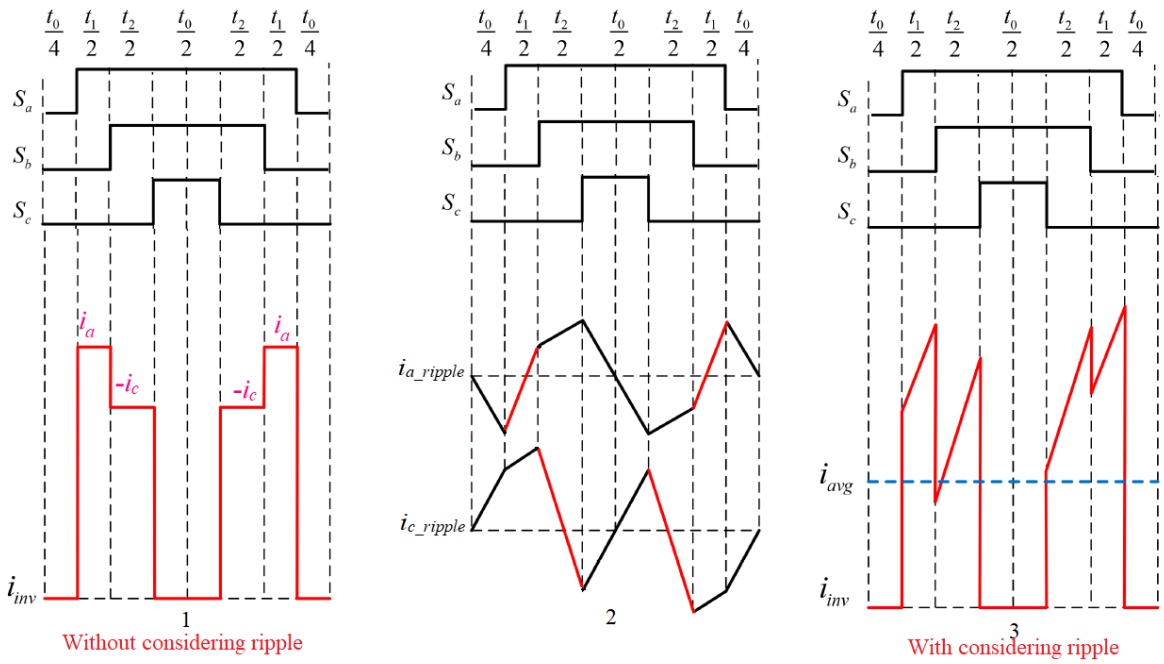

Fig. 9. DC-link current in a switching cycle under SVM switching in first sextant.

Equation (8) shows the DC-link capacitor current caused by load current ripple can be calculated as follows [9]:

$$i^2_{ripple,rms,SVPWM} = \frac{3\sqrt{3}m^3v^2_{dc}}{64\pi L^2 f_s^2}\left\{\left[\frac{91}{80}k_z^2 - \frac{91}{80}k_z + \frac{179}{480}\right]m^2 + \left[-\left(\frac{\sqrt{3}}{3}\pi + \frac{15}{16}\right)k_z^2 + \left(\frac{\sqrt{3}}{3}\pi + \frac{15}{16}\right)k_z - \frac{3}{32} - \frac{7\sqrt{3}}{48}\pi\right]m + \left(\frac{5}{3}k_z^2 - \frac{5}{3}k_z + \frac{29}{54}\right)\right\} \quad (8)$$

where m is modulation index, f_s is switching frequency, L is converter side inductor, and k_z is coefficient of zero vector distribution.

As (8) shows, this component of the DC-link capacitor's current is inversely proportional to the switching frequency. Therefore, increasing switching frequency can significantly reduce this component of the DC-link current.

Benefits of Increased Switching Frequency on DC-Link Capacitors

When designing a DC-link capacitor for an inverter, the ripple current requirement typically ends up being the limiting factor. As ripple current induces power dissipation due to ESR, the generated heat results in greater stress, leading to reduced service life of the entire inverter. This is a key

consideration particularly when selecting electrolytic capacitors as they have relatively high ESR, perhaps necessitating many in parallel to stay within specific ripple limits.

As previously stated, high switching frequency reduces ripple current. This reduction of ripple current reduces losses in the capacitors. Fewer losses means smaller rise in core temperature which yields longer component life, more reliability and slightly better efficiency on the DC-link. It also may reduce volume and weight, in the case that capacitors are paralleled to endure high ripple current.

Additionally, as stated in Table. I and (8), the capacitor overall voltage ripple due to constant and variant parts of the current in a switching interval is proportional to T_s ($1/f_s$) and T_s^2 ($1/f_s^2$), *respectively*. Therefore, for a defined maximum voltage ripple, as f_s increases, capacitor size reduces drastically and leads to weight, volume and cost reduction, and an increase in power density. Also, alternatively, higher-performance capacitor material such as film becomes an option, bringing even greater performance and reliability. Film capacitors have a considerably longer lifespan than electrolytics, stable operation over a wide range of temperatures, momentary overvoltage withstand, extremely long shelf life, lower ESR and mechanical robustness. All these factors help in the manufacturing, utilization and maintenance stages.

Until recently, higher switching frequency has been impossible to achieve due to unwanted side effects such as increased switching losses and EMI as well as reduced reliability. With the Hillcrest high-efficiency inverter technology, which materially eliminates switching losses and reduces EMI, the desired increased switching frequency is achievable. Therefore, the benefits of increased switching frequency on DC-link capacitors can be exploited without sacrificing other factors such as the efficiency of the inverter and electromagnetic compatibility (EMC).

Simulation and Experimental Results

A simulation was conducted to verify and evaluate the effect of increased switching frequency on DC-link capacitor ripple current. In these simulations, circuit parameters remain the same and only the switching frequency was varied; 10kHz for the first case and 30kHz for the second. The results are shown in Figs. 10 and 11. As illustrated, the ripple current of the DC-link capacitors is considerably lower in the case with the higher switching frequency, which results in smaller DC-link capacitor size, cost and/or a longer capacitor useful life.

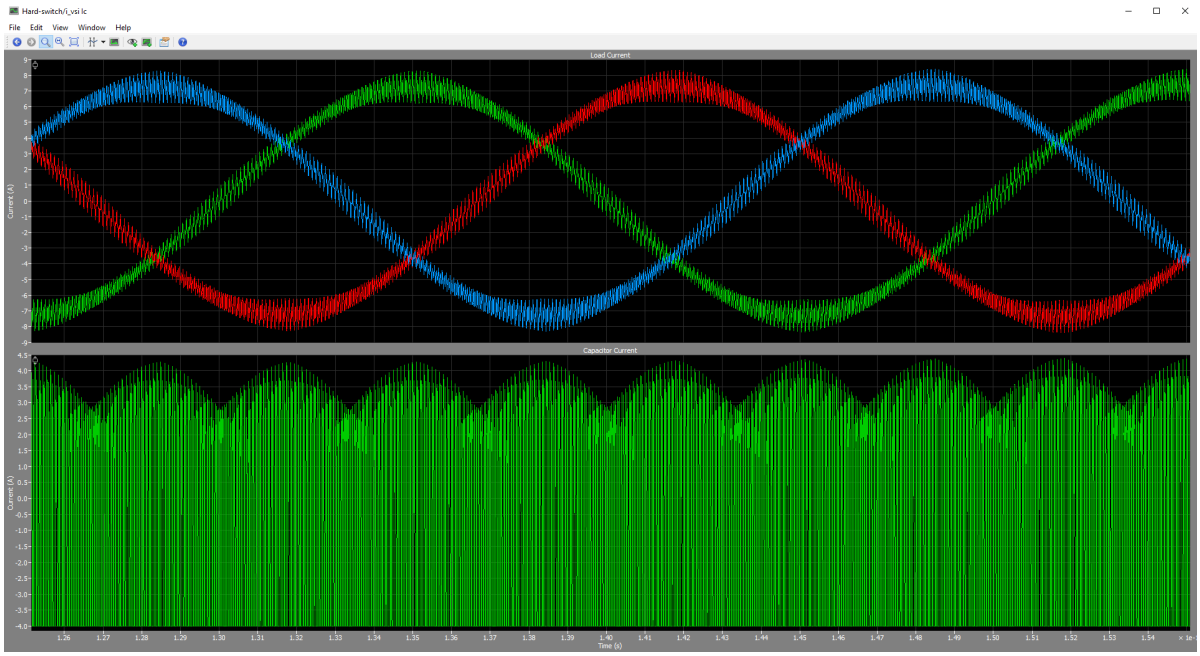

Fig. 10. DC-link capacitor's current of the simulated converter with 10kHz switching frequency.

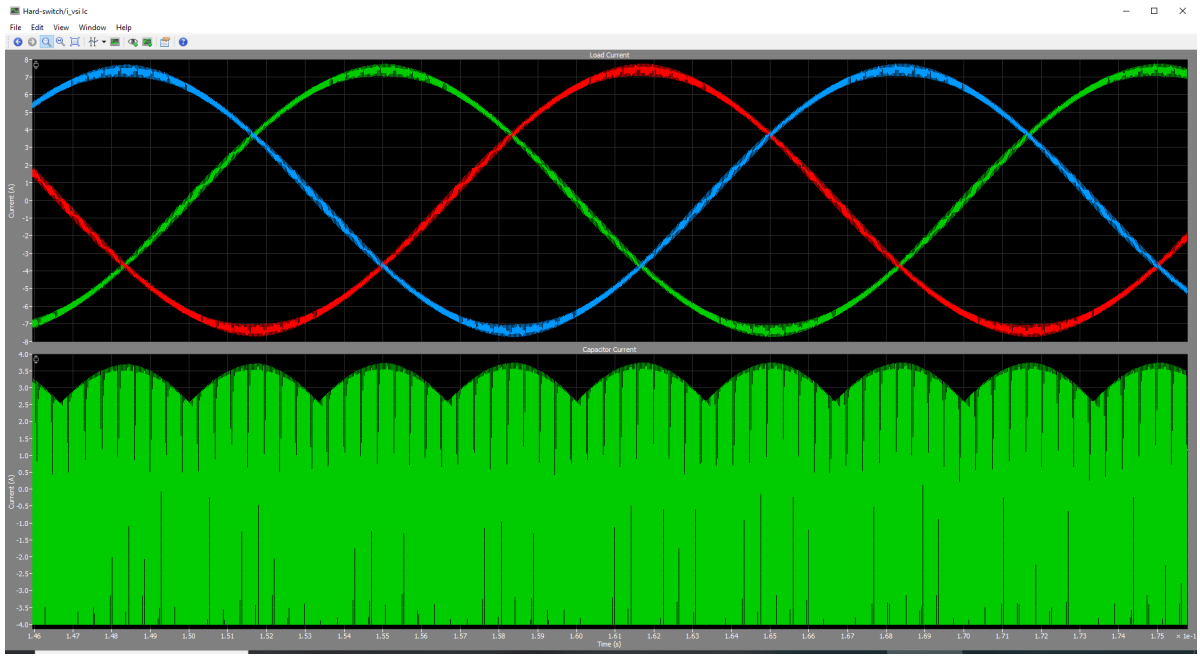

Fig. 11. DC- link capacitor's current of the simulated converter with 30kHz switching frequency.

Next, to demonstrate empirically, a test with resistive-inductive load was performed as per the simulation: 10kHz for the first case and 30kHz for the second. The results are shown in Fig. 12 through Fig. 15. In accordance with the simulation results, the capacitor ripple current is considerably lower when the switching frequency is higher. In addition, The RMS value of the

capacitor current (encircled in red in Figs. 12 and 13) in the 30kHz case is lower than in the 10kHz case.

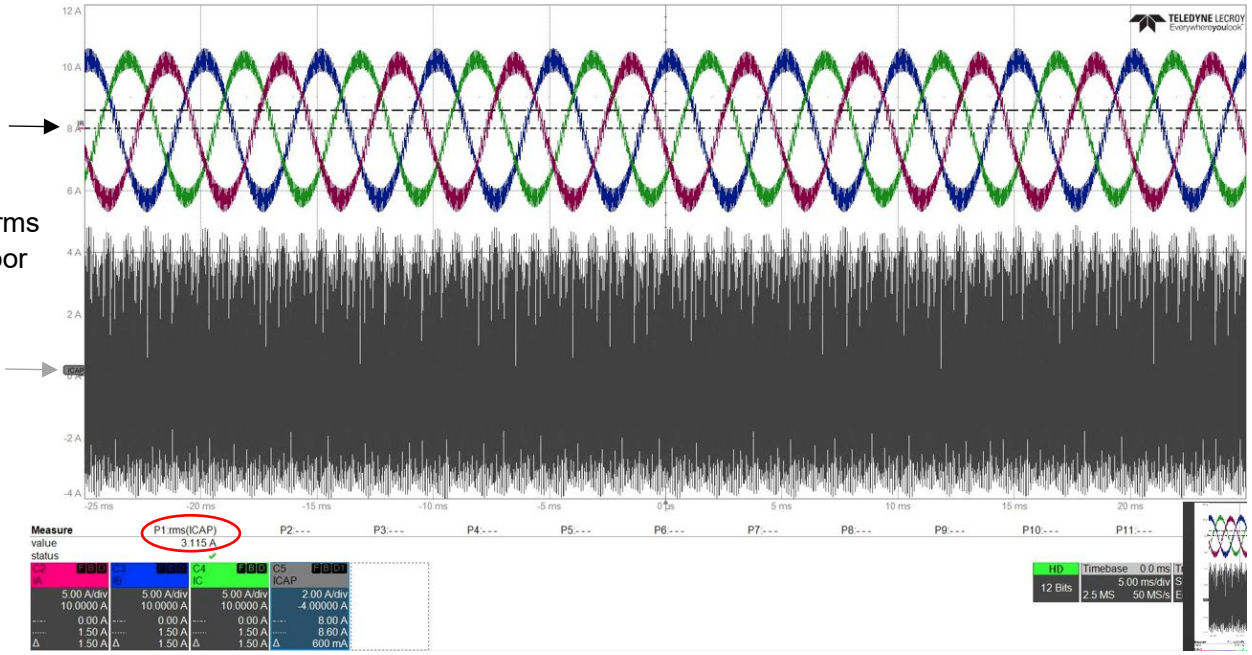

Fig. 12. Phase currents and DC link capacitor's current of the converter with 10kHz switching frequency.

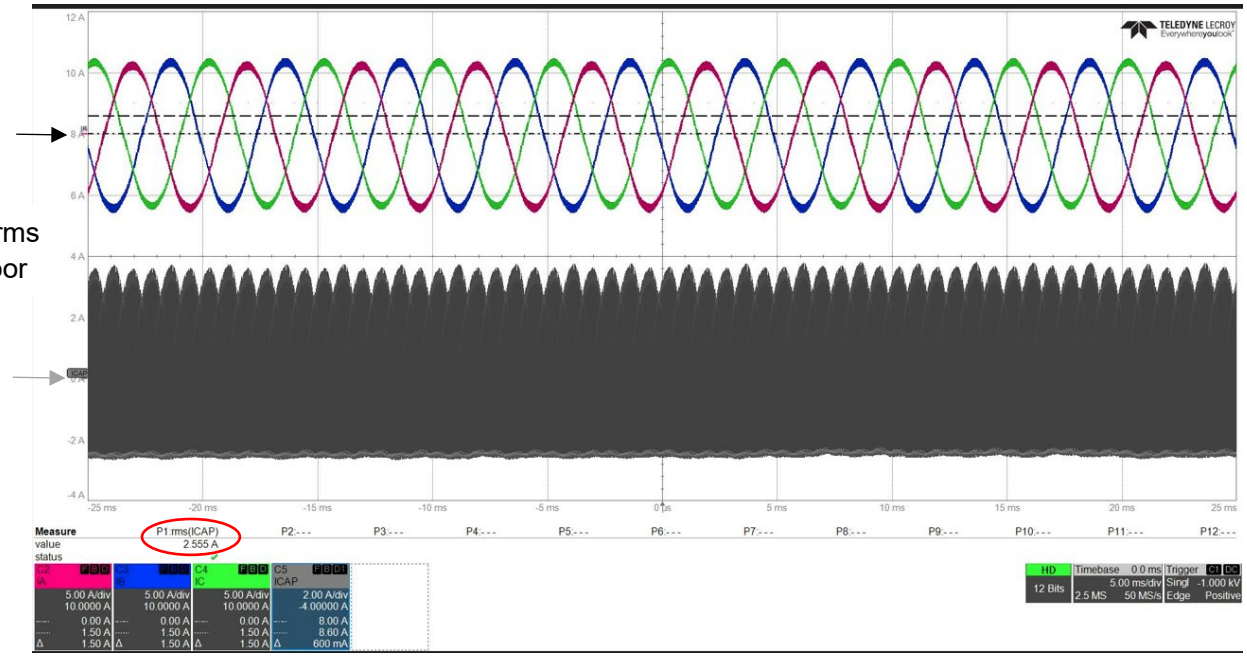

Fig. 13. Phase currents and DC link capacitor's current of the converter with 30kHz switching frequency.

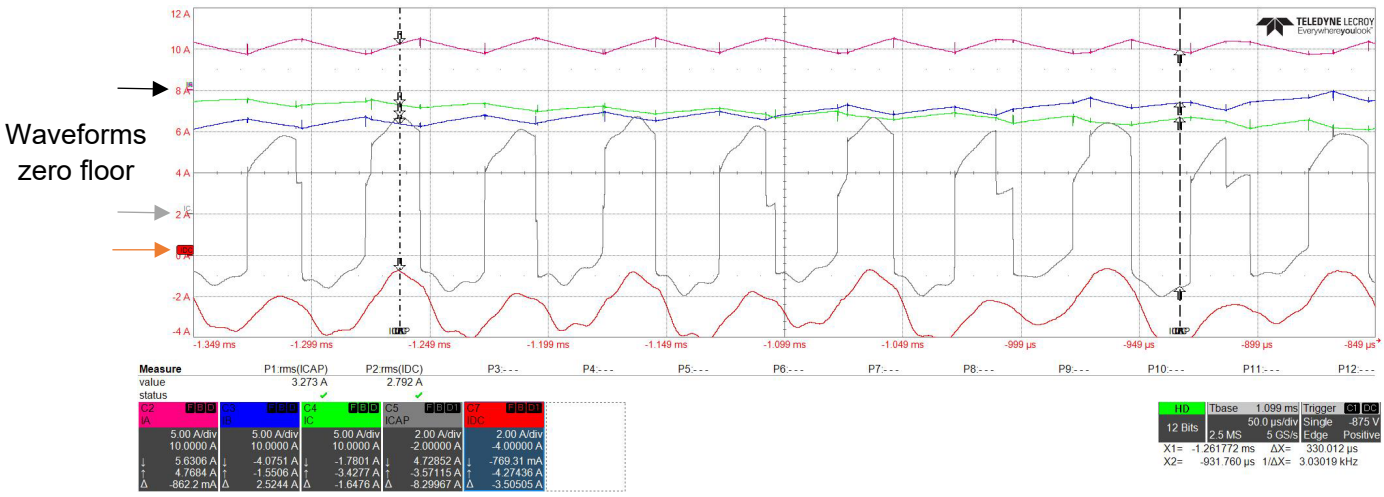

Fig. 14. Zoomed phase currents and DC link capacitor's current of the converter with 10kHz switching frequency.

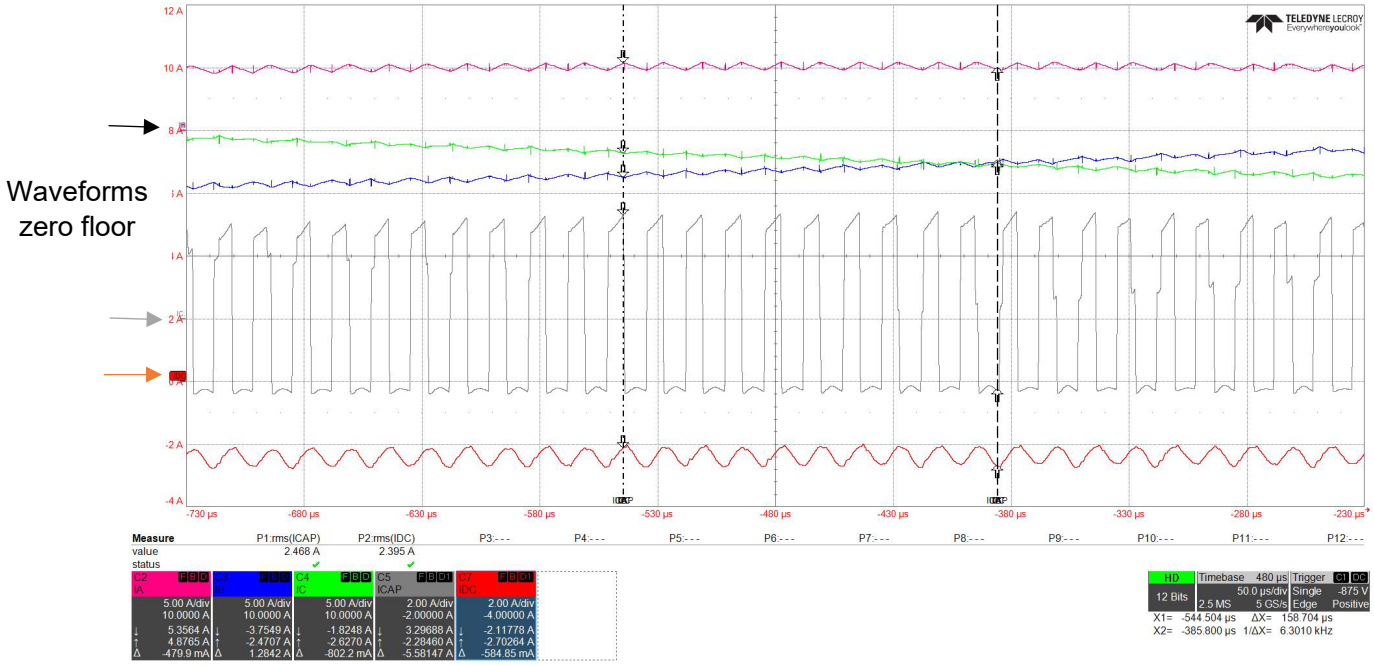

Fig. 15. Zoomed phase currents and DC link capacitor's current of the converter with 30kHz switching frequency.

As Figs. 16 and 17 illustrate, higher switching frequency also reduces oscillating current at the DC-source side. As frequency increases, the DC source and cable parasitic inductance cause the impedance in the power source/battery path to increase. The DC-link capacitor impedance goes down. Therefore, it becomes the preferable path for high-frequency current to circulate, further reducing the DC-source current ripple.

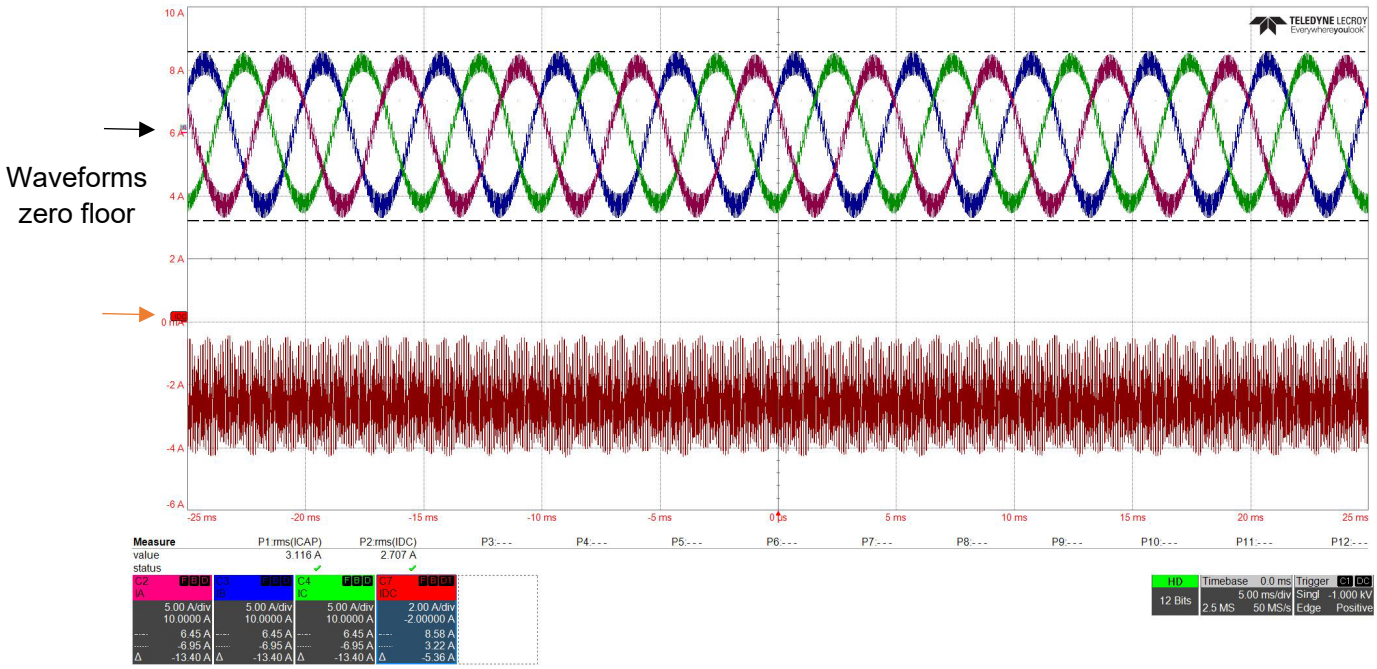

Fig. 16. Phase and DC-source currents of the converter with 10kHz switching frequency.

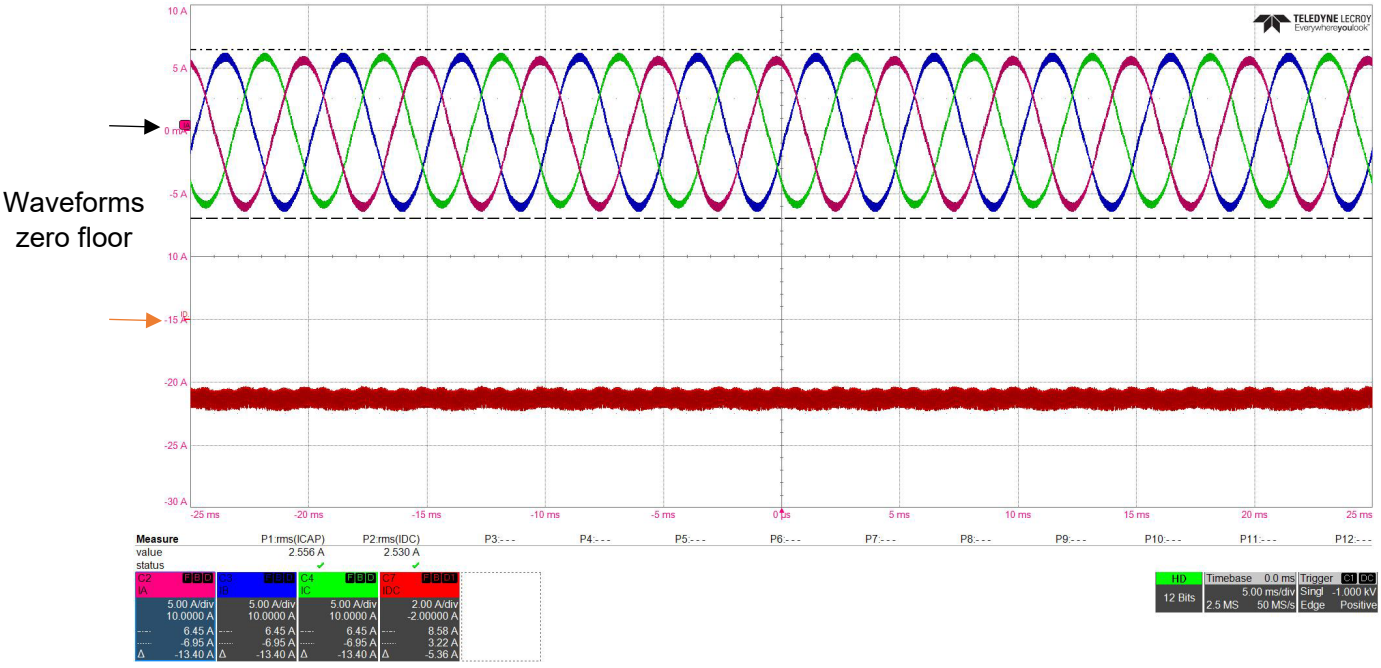

Fig. 17. Phase and DC-source currents of the converter with 30kHz switching frequency.

Fig. 18 compares the frequency spectrum of the DC-source current in both test cases. Higher switching frequency reduces harmonic magnitude, especially in lower orders. Therefore, a higher switching frequency can result in longer battery life and a smaller filter on the DC side.

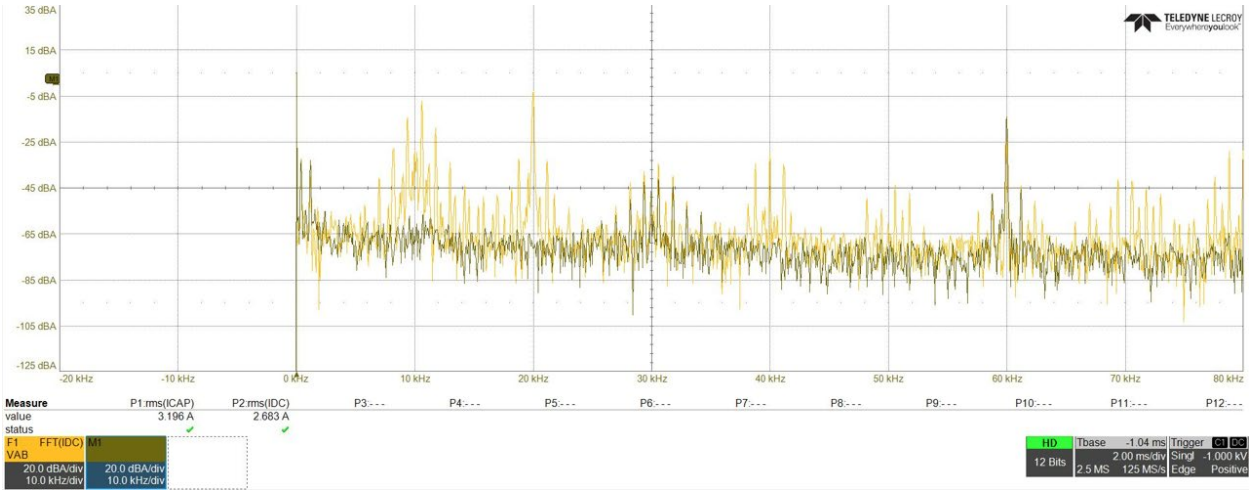

Fig. 18. Comparison of frequency spectrum of the DC-source current (dark yellow - 30kHz; bright yellow -10kHz).

Table II compares results for each test case. As outlined in the comparison, higher switching frequency has beneficial effects on both the DC-link capacitor and DC source. Decreased charging/discharging interval and a reduction in peak ripple current combine to make it possible to reduce capacitor size.

Table. II: Comparison of the effect of switching frequency on DC-link parameters.

Parameter	10kHz	30kHz	Improvement 30kHz vs. 10kHz
Peak to peak capacitor current ripple	8.7A	5.6A	35.6%
RMS capacitor ripple current	3.2A	2.5A	21.9%
Peak to peak capacitor voltage ripple	9.5V	1.9V	80.0%
Peak to peak DC source current ripple	3.8A	0.7A	81.6%
RMS DC source current	2.7A	2.5A	7.4%
DC-source ripple current harmonic content	High - especially at lower frequency	Low - especially at lower frequency (refer to Fig. 8)	

Conclusion

The positive impact of higher switching frequency on DC-link capacitor design has been demonstrated. Simulation and experimental results have shown that higher switching frequencies indeed reduce DC-link capacitor ripple current. Given that the ESR of a given capacitor type reduces with frequency (approaching 100kHz), and that power loss and temperature rise are dependent on ESR, internal thermal rise is reduced. This leads to longer component life and more reliability along with higher efficiency. Ripple current reduction can also result in volume, weight and cost reductions, as fewer parallel capacitors are need to meet manufacturer ripple limits. Moreover, the DC-link capacitor size is inversely proportional to switching frequency. As switching frequency increases, the required capacitance decreases. Capacitor volume is proportional to capacitance; therefore, with increased switching frequency, higher power density and lower cost can be achieved.

Increasing switching frequencies traditionally come at costs such as additional switching losses, increased EMI and reduced reliability. The key to accessing such beneficial higher frequencies requires a technological leap that addresses these existing barriers. Hillcrest's soft-switching technology enables these higher switching frequencies whilst mitigating switching losses and reducing electromagnetic compatibility issues.

References

[1] Chris Whaling, “EV Power Electronics Cost Analysis” IEEE Transportation Electrification Community (TEC) eNewsletter, May/June 2014.

[2] A. Nordelöf, M.Alatalo, M. L. Söderman “A scalable life cycle inventory of an automotive power electronic inverter unit—part I: design and composition,” The International Journal of Life Cycle Assessment, vol. 24, 2019, pp. 78–92.

[3] S. Yang, A. Bryant, P. Mawby, D. Xiang, L. Ran, P. Tavner, “An industry-based survey of reliability in power electronic converters,” IEEE Trans. Ind. Appl. vol. 47, no. 3, March 2011, pp. 1441–1451.

[4] A. Golnas, "PV System Reliability: An Operator's Perspective," in IEEE Journal of Photovoltaics, vol. 3, no. 1, pp. 416-421, Jan. 2013, doi: 10.1109/JPHOTOV.2012.2215015.

[5] F. D. Kieferndorf, M. Forster and T. A. Lipo, "Reduction of DC-bus capacitor ripple current with PAM/PWM converter," in *IEEE Transactions on Industry Applications*, vol. 40, no. 2, pp. 607-614, March-April 2004.

[6] TDK Film Capacitors General technical information, Available at: https://www.tdk-electronics.tdk.com/download/530754/480aeb04c789e45ef5bb9681513474ba/pdf-generaltechnicalinformation.pdf

[7] H. Wang and F. Blaabjerg, "Reliability of Capacitors for DC link Applications in Power Electronic Converters—An Overview," in IEEE Transactions on Industry Applications, vol. 50, no. 5, pp. 3569-3578, Sept.-Oct. 2014, doi: 10.1109/TIA.2014.2308357.

[8] Q. Li, D. Jiang, “DC link current analysis of three-phase 2L-VSI considering AC current ripple,” IET Power Electron., vol. 11, no. 1, pp. 202-211, 2018.

[9] T. Wang, S. Lu, “DC link current computational methods for three-phase inverter with low-order harmonic output current,” IET Power Electron., vol. 12, no. 4, pp. 878-890, 2019.